ABSTRACT OF THE DISCLOSURE

Methods of forming dynamic random access memories (DRAM) are described. In one embodiment, an insulative layer is formed over a substrate having a plurality of conductive lines which extend within a memory array area and a peripheral area outward of the memory array. Capacitor container openings and contact openings are contemporaneously etched over the memory array and conductive line portions within the peripheral area respectively. In another embodiment, a patterned masking layer is formed over a substrate having a plurality of openings formed within an insulative layer, wherein some of the openings comprise capacitor container openings within a memory array and other of the openings comprise conductive line contact openings disposed over conductive lines within a peripheral area outward of the memory array. With a common patterned masking layer, unmasked portions of a capacitor electrode layer are removed within the memory array and material from over portions of the conductive lines within the peripheral area is removed sufficient to expose conductive material of the conductive line portions. In yet another embodiment, a common etch chemistry is used to remove selected material of an insulative material layer formed over conductive lines within a peripheral area and material of a storage capacitor electrode layer. In yet another embodiment, a plurality of conductive plugs are formed over substrate node locations over which storage capacitors are to be formed. After forming the

plugs, insulative material over conductive lines within a peripheral area is removed to first expose conductive material of the conductive lines.